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What is claimed is:

1. An integrated circuit timing circuit comprising:

a programmable non-volatile fuse circuit; and

an adjustable delay element coupled to the programmable non-volatile fuse circuit, the delay element has a plurality of propagation times selectable in response to the programmable non-volatile fuse circuit.

2. The integrated circuit timing circuit of claim 1 further comprising a volatile latch circuit coupled between the programmable non-volatile fuse circuit and the adjustable delay element.

3. The integrated circuit timing circuit of claim 1 wherein the programmable non-volatile fuse circuit comprises a plurality of flash memory cells.

4. The integrated circuit timing circuit of claim 1 further comprises a set/reset latch coupled to an output of the adjustable delay element.

5. The integrated circuit timing circuit of claim 1 wherein the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path in response to the programmable non-volatile fuse circuit to establish one of the plurality of propagation times.

6. An integrated circuit timing circuit comprising:

a programmable non-volatile fuse circuit;

a volatile latch circuit coupled to the non-volatile fuse circuit; and

a plurality of adjustable delay elements coupled to the volatile latch circuit, each of the plurality of adjustable delay elements comprises a propagation path, and a plurality of capacitors selectively coupled to the propagation paths of the plurality of adjustable delay elements in response to the volatile latch circuit.

7. The integrated circuit timing circuit of claim 6 wherein the plurality of capacitors selectively coupled to the propagation paths via a switch activated by the volatile latch circuit.

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8. The integrated circuit timing circuit of claim 6 further comprising:

logic circuitry coupled to an input of the plurality of adjustable delay elements; and

latch circuitry coupled to an output of the plurality of adjustable delay elements.

9. A memory device comprising:

an array of memory cells;

access circuitry to generate a plurality of memory array access signals; and

an adjustable timing circuit coupled to the access circuitry, the adjustable timing circuit comprises,

a programmable non-volatile fuse circuit, and

an adjustable delay element coupled to the programmable non-volatile fuse circuit, the delay element has a plurality of propagation times selectable in response to the programmable non-volatile fuse circuit.

10. The memory device of claim 9 further comprising a volatile latch circuit coupled between the programmable non-volatile fuse circuit and the adjustable delay element.

11. The memory device of claim 9 wherein the programmable non-volatile fuse circuit comprises a plurality of flash memory cells.

12. The memory device of claim 9 wherein the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path in response to the programmable non-volatile fuse circuit to establish one of the plurality of propagation times.

13. A synchronous flash memory device comprising:

an array of non-volatile memory cells;

access circuitry to generate a plurality of memory array access signals; and

an adjustable timing circuit coupled to the access circuitry, the adjustable timing circuit comprises,

a programmable non-volatile fuse circuit comprising non-volatile memory cells,

a volatile latch circuit coupled to the non-volatile fuse circuit, and

a plurality of adjustable delay elements coupled to the volatile latch circuit, each of the plurality of adjustable delay elements comprises a propagation path, and a plurality of capacitors selectively coupled to the propagation paths of the plurality of adjustable delay elements in response to the volatile latch circuit.

14. The flash memory of claim 13 wherein the plurality of capacitors selectively coupled to the propagation paths via a switch activated by the volatile latch circuit.

15. A method of adjusting a signal timing circuit comprising:

programming a non-volatile fuse circuit; and

selecting a signal propagation time length in response to the programmed non-volatile fuse circuit.

16. The method of claim 15 wherein selecting the signal propagation time length comprises selectively coupling one or more capacitors to a propagation path of the signal timing circuit.

17. The method of claim 15 wherein the non-volatile fuse circuit comprises a plurality of floating gate transistors.

18. The method of claim 15 further comprises storing data from the non-volatile fuse circuit in a plurality of volatile latches.

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19. A method of adjusting a signal timing circuit comprising:

programming a plurality of non-volatile fuses to store first data;

copying the first data from the plurality of non-volatile fuses to a plurality of latch circuits; and

selecting a signal propagation time length in response to the first data stored in the plurality of latch circuits.

20. The method of claim 19 wherein the wherein selecting the signal propagation time length comprises selectively coupling one or more capacitors to a propagation path of the signal timing circuit.

21. The method of claim 19 wherein the non-volatile fuse circuit comprises a plurality of floating gate transistors.

22. A method of testing a memory device comprising a signal propagation path, the method comprises:

programming a plurality of non-volatile fuses to store first data;

selectively coupling one or more capacitors to the propagation path in response to the first data to provide a first propagation path delay time;

testing the memory using the first propagation path delay time;

programming the plurality of non-volatile fuses to store second data;

selectively coupling one or more capacitors to the propagation path in response to the second data to provide a second propagation path delay time; and

testing the memory using the second propagation path delay time.

23. The method of claim 22 wherein the memory device is a flash memory having an array of floating gate memory cells and the plurality of non-volatile fuses comprise floating gate transistors.

24. The method of claim 22 further comprising:

copying the first data from the plurality of non-volatile fuses to a plurality of latches before selectively coupling one or more capacitors to the propagation path in response to the first data; and

copying the second data from the plurality of non-volatile fuses to the plurality of latches before selectively coupling one or more capacitors to the propagation path in response to the second data.